UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,514	03/09/2004	John P. Snyder	14467.05	1961

7590 01/07/2008

David J King
Spinnaker Semiconductor, Inc.
3769 Wescott Hills Drive
Eagan, MN 55123

EXAMINER	
KIM, SU C	

ART UNIT	PAPER NUMBER
2823	

MAIL DATE	DELIVERY MODE
01/07/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/796,514	SNYDER ET AL.	
	Examiner	Art Unit	
	Su C. Kim	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-21,23-31 and 33-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-21,23-31 and 33-65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. PCT/US02/25289.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/07/2007 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1- 8, 10-21, 23-31, & 33-65 are rejected under 35 U.S.C. 102(e) as being anticipated by Yu et al. (US 6,894,355)

Regarding claims 1, 15, & 24, Yu discloses a method for manufacture of a device for regulating the flow of electrical current, the method comprising:

providing for a semiconductor substrate 18 (Fig. 3A);

providing for an electrical insulating layer 64 (Fig. 3A, col. 4, lines 63-67, note: buffer layer 62 can be omitted) in contact with the semiconductor substrate 18 , the insulating layer having a dielectric constant greater than 4.0, 7.5, or 15 (col. 5, table 1);

providing for a gate electrode 28 in contact with at least a portion of the insulating layer 64 (Fig. 3A); and

providing a source electrode 20 and a drain electrode 22 in contact with the semiconductor layer 18 (Fig. 3C, col. 6 lines 42-54) and proximal to the gate electrode 28 wherein a channel is formed between the source and drain electrode, and further wherein at least one of source electrode and the drain electrode forms a Schottky contact or Schottky-like region 20 & 22 (Fig. 3C) with the semiconductor substrate and the channel (Fig. 3C, col. 6 lines 42-54) .

Regarding claims 2, 16, & 25, as applied to claims 1, 15, & 24, Yu discloses that the source and drain electrode are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide (Col. 6, lines 37-40).

Regarding claims 3, 17, & 26, as applied to claims 1, 15, & 24, Yu discloses that the source and drain electrodes are formed from a member of the group consisting of the rare earth silicide (Col. 6, lines 37-40).

Regarding claims 4, 18, & 27, as applied to claims 1, 15 & 24, Yu discloses that insulating layer is formed from a member of the group consisting of metal oxide (Col. 5, table 1).

Regarding claims 5, 19, & 28, as applied to claims 1, 15 & 24, Yu discloses that insulating layer is formed from a member of the group consisting of oxy-nitride stack (Col. 5, table 1).

Regarding claims 6, 20, & 29, as applied to claims 1, 15 & 24, Yu discloses that the Schottky contact or Schottky-like region 20 & 22 is formed at least in areas adjacent to the channel (Fig. 3C).

Regarding claims 7, 21, & 30, as applied to claims 1, 15 & 24, Yu discloses that an entire interface between at least one of the source electrode 20 and the drain electrode 22 and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate 18 (Fig. 3C).

Regarding claims 8, 23, & 31, as applied to claims 1, 15 & 24, Yu discloses that dopants are introduced into the channel (Col. 7, lines 5-7).

Regarding claims 10, as applied to claims 2 or 3, Yu discloses that insulating layer is formed from a member of the group consisting of metal oxide (Col. 5, table 1).

Regarding claim 11, as applied to claims 2 or 3, Yu discloses that insulating layer is formed from a member of the group consisting of oxy-nitride stack (Col. 5, table 1).

Regarding claim 12, as applied to claim 10, Yu discloses that dopants are introduced into the channel (Col. 7, lines 5-7).

Regarding claim 13, as applied to claim 11, Yu discloses that dopants are introduced into the channel (Col. 7, lines 5-7).

Regarding claim 14, as applied claims 2 or 3, Yu discloses providing a source electrode and a drain electrode in contact with the semiconductor substrate 18 is performed at a processing temperature of less than 800 °C (Col. 6, 51-55).

Regarding claim 33, 44, & 55, Yu discloses that a method for manufacture of a device for regulating the flow of electrical current, the method comprising:

providing for a semiconductor substrate 18 (Fig. 3A);

providing for an electrically insulating layer 64 in contact with the semiconductor substrate 18 (Fig. 3A), the insulating layer having a dielectric constant greater than 4, 7.6, or 15 (Col. 5, Table 1);

providing for a gate electrode 28 locating in contact with at least a portion of the insulating layer 64 (Fig. 3A);

exposing the semiconductor substrate 18 on one or more areas proximal to the gate electrode 28 (Fig. 3A, col6, lines 18-21);

providing for a thin film of metal 74 on at least a portion of the exposed semiconductor substrate 18 (Fig. 3B); and

reacting the metal 74 with the exposed semiconductor substrate 18 such that a source electrode 20 and a drain electrode 22 are formed and wherein a channel is formed between the source electrode and the drain electrode, and further wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region 20 & 22 with the semiconductor substrate and the channel 18 (Fig. 3C).

Regarding claims 34, 45, & 56, as applied to claims 33, 44, & 55, Yu discloses that the gate electrode is provide by:

disposing a thin conductive film to form a gate electrode 28(Fig. 3A); and forming one or more thin insulating layers 30 on one or more side walls 34 of the gate electrode (Fig. 3B).

Regarding claims 35, 46, & 57, as applied to claims 33, 44, & 55, Yu discloses that removing metal not reacted during the reacting process (Fig. 3C).

Regarding claims 36, 47, & 58, as applied to claims 33, 44, & 55, Yu discloses the reacting comprising thermal annealing (Col. 6, lines 53-54).

Regarding claims 37, 48, & 59, as applied to claims 33, 44, & 55, Yu discloses that the source and drain electrode are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide (Col. 6, lines 37-40).

Regarding claims 38, 49, & 60, as applied to claims 33, 44, & 55, Yu discloses that the source and drain electrodes are formed from a member of the group consisting of the rare earth silicide (Col. 6, lines 37-40).

Regarding claims 39, 50, & 61, as applied to claims 33, 44, & 44, Yu discloses that insulating layer is formed from a member of the group consisting of metal oxide (Col. 5, table 1).

Regarding claims 40, 51, & 62, as applied to claims 33, 44, & 44, Yu discloses that insulating layer is formed from a member of the group consisting of oxy-nitride stack (Col. 5, table 1).

Regarding claims 41, 52, & 63, as applied to claims 33, 44, & 44Yu discloses that the Schottky contact or Schottky-like region 20 & 22 is formed at least in areas adjacent to the channel (Fig. 3C).

Regarding claims 42, 53, & 64, as applied to claims 33, 44, & 44, Yu discloses that an entire interface between at least one of the source electrode 20 and the drain electrode 22 and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate 18 (Fig. 3C).

Regarding claims 43, 54, & 65, as applied to claims 33, 44, & 44, Yu discloses that dopants are introduced into the channel (Col. 7, lines 5-7).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Su C. Kim whose telephone number is (571) 272-5972. The examiner can normally be reached on Monday - Thursday, 9:00AM to 7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Su C Kim
Examiner
Art Unit 2823

12/31/2007

PRIMARY EXAMINER
WILLIAM DAVID COLEMAN